IN THE CLAIMS:

1. (currently amended) A data processing system comprising:

a memory for storing operands;

at least one general purpose register; and

processor circuitry for executing one or more instructions, a first single instruction of the one or more instructions for transferring data elements between the memory and the at least one general purpose register wherein ~~the~~ the first single instruction specifies both a size of data elements in the memory and a size of data elements in the at least one general purpose register, wherein the size of data elements in memory, as specified by the first single instruction, is separate and independent from the size of data elements in the at least one general purpose register, as specified by the first single instruction ~~the first single instruction specifies the size of the data elements in memory separate and independent from specifying the size of the data elements in the at least one general purpose register~~.

2. (previously presented) The data processing system of claim 1 wherein the first single instruction comprises independent fields for separately storing a first data size specifier for the memory and a second data size specifier for the at least one general purpose register.

3. (previously presented) The data processing system of claim 1 wherein the first single instruction specifies a storage location for defining a first data size specifier for the memory and a second data size specifier for the at least one general purpose register.

4. (original) The data processing system of claim 3 wherein the storage location is any one of a location in the memory and a processor register location external to the memory.

5. (original) The data processing system of claim 3 wherein the storage location is a control register of the data processing system.

6. (original) The data processing system of claim 3 wherein the storage location is a register within the data processing system that arithmetic, logical and shift operations performed by the data processing system utilize.

7. (original) The data processing system of claim 1 wherein the memory further comprises a plurality of multiple data elements to be transferred between the memory and the at least one general purpose register.

8. (original) The data processing system of claim 7 wherein the multiple data elements are contiguous in the memory.

9. (original) The data processing system of claim 7 wherein the multiple data elements are non-contiguous in the memory.

10. (original) The data processing system of claim 1 wherein each of the at least one general purpose register holds multiple data elements.

11. (original) The data processing system of claim 1 wherein each of the at least one general purpose register comprises a scalar register that has a one-dimensional memory map.

12. (previously presented) The data processor of claim 1 wherein when the first single instruction specifies size of a source data element in the memory to be greater than size of a destination data element in the at least one general purpose register, the processor circuitry truncates a portion of the source data element in the memory.

13. (original) The data processor of claim 12 wherein the portion of the source data element in the memory that is truncated is a high order portion of the source data element in the memory.

14. (original) The data processor of claim 12 wherein the portion of the source data element in the memory that is truncated is a low order portion of the source data element in the memory.

15. (previously presented) The data processor of claim 1 wherein when the first single instruction specifies size of a source data element in the memory to be greater than the size of a destination data element in the at least one general purpose register, the processor circuitry rounds a high order portion of the source data element in the memory based on a value of a low order portion of the source data element in the memory.

16. (previously presented) The data processor of claim 1 wherein when the first single instruction specifies size of a source data element in the memory to have a smaller size than a destination data element in the at least one general purpose register, the processor circuitry places predetermined data values in a portion of the destination data element of the at least one general purpose register that is not filled by the source data element from the memory.

17. (original) The data processor of claim 16 wherein the processor circuitry places predetermined data values in the portion of the destination data element of the at least one general purpose register by using zero extension.

18. (original) The data processor of claim 16 wherein the processor circuitry places predetermined data values in the portion of the destination data element of the at least one general purpose register by using sign extension.

19. (original) The data processor of claim 16 wherein the processor circuitry places predetermined data values in the portion of the destination data element of the at least one general purpose register by filling a predetermined bit value in a low order data portion of the destination data element of the at least one general purpose register.

20. (original) The data processor of claim 19 wherein the predetermined bit value is a zero value.

21. (previously presented) The data processor of claim 1 wherein when the first single instruction specifies size of a destination data element in the memory to be less than a size of a source data element in the at least one general purpose register, the processor circuitry truncates a portion of the source data element in the at least one general purpose register.

22. (original) The data processor of claim 21 wherein the processor circuitry truncates a high order portion of the source data element in the at least one general purpose register.

23. (original) The data processor of claim 21 wherein the processor circuitry truncates a 10 low order portion of the source data element in the at least one general purpose register.

24. (previously presented) The data processor of claim 1 wherein when the first single instruction specifies size of a destination data element in the memory to be less than a size of a source data element in the at least one general purpose register, the processor circuitry rounds a high order portion of the source data element in the at least one general purpose register based on a value of a low order portion of the source data element.

25. (previously presented) The data processor of claim 1 wherein when the first single instruction specifies size of a destination data element in the memory to be greater than a size of a source data element in the at least one general purpose register, the processor circuitry places predetermined data values in a portion of the destination data element in the memory that is not filled by the source data element in the at least one general purpose register.

26. (original) The data processor of claim 25 wherein the processor circuitry places the predetermined data values in the portion of the destination data element in the memory that is not filled by using zero extension.

27. (original) The data processor of claim 25 wherein the processor circuitry places the predetermined data values in the portion of the destination data element in the memory that is not filled by using sign extension.

28. (original) The data processor of claim *25* wherein the processor circuitry places the predetermined data values in the portion of the destination data element in the memory that is not filled by placing a predetermined bit value in a low order data portion of the destination data element.

29. (original) The data processor of claim 28 wherein the predetermined bit value is zero.

30. (currently amended) A method for loading and storing data elements in a data processing system comprising:

providing a memory for storing operands;

providing at least one general purpose register; and

executing one or more instructions, a first single instruction causing a transfer of data elements between the memory and the at least one general purpose register wherein the first single instruction specifies both a size of data elements in the memory and a size of data elements in the at least one general purpose register, wherein the size of data elements in memory, as specified by the first single instruction, is separate and independent from the size of data elements in the at least one general purpose register, as specified by the first single instruction ~~the first single instruction specifies the size of the data elements in the memory separate and independent from specifying the size of the data elements in the at least one general purpose register~~.

31. (previously presented) The method of claim 30 further comprising:

specifying size of data elements by implementing independent fields within the first single instruction, a first field indicating a first data size specifier for the memory and a second field indicating a second data size specifier for the at least one general purpose register.

32. (previously presented) The method of claim 30 further comprising:

specifying size of data elements by implementing a predetermined field within the first single instruction, the predetermined field indicating a storage location for

defining a first data size specifier for the memory and a second data size specifier for the at least one general purpose register.

33. (original) The method of claim 30 further comprising:
implementing the multiple data elements in contiguous storage within the memory.

34. (original) The method of claim 30 further comprising:
implementing the multiple data elements in non-contiguous storage within the memory.

35. (previously presented)) The method of claim 30 further comprising:
truncating a portion of a source data element in the memory when the first single instruction specifies size of the source data element in the memory to be greater than size of a destination data element in the at least one general purpose register.

36. (previously presented) The method of claim 30 further comprising:
rounding a high order portion of a source data element in the memory based on a value of a low order portion of the source data element in the memory when the first single instruction specifies size of the source data element in the memory to be greater than a size of a destination data element in the at least one general purpose register.

37. (previously presented) The method of claim 30 further comprising:
placing predetermined data values in a portion of a destination data element of the at least one general purpose register that is not filled by a source data element from the memory when the first single instruction specifies a size of the source data element in the memory to have a smaller size than the destination data element in the at least one general purpose register.

38. (previously presented) The method of claim 30 further comprising:

truncating a portion of a source data element in the at least one general purpose register when the first single instruction specifies size of a destination data element in the memory to be less than a size of the source data element in the at least one general purpose register.

39. (previously presented) The method of claim 30 further comprising:

rounding a high order portion of a source data element in the at least one general purpose register based on a value of a low order portion of the source data element when the first single instruction specifies size of a destination data element in the memory to be less than a size of the source data element in the at least one general purpose register.

40. (previously presented) The method of claim 30 further comprising:

placing predetermined data values in a portion of a destination data element in the memory that is not filled by a source data element in the at least one general purpose register when the first single instruction specifies size of the destination data element in the memory to be greater than a size of the source data element in the at least one general purpose register.

41. (previously presented) A data processing system comprising a memory and a processor for executing data processing instructions, a first single instruction of the data processing instructions comprises control information that specifies both a size of data elements stored in the memory and a size of data elements stored in at least one storage location in the data processing system external to the memory, wherein the first single instruction specifies the size of the data elements stored in the memory separate and independent from specifying the size of the data elements stored in the at least one storage location in the data processing system external to the memory.

42. (previously presented) The data processing system of claim 41 wherein the control information of the first single instruction of the data processing instructions further comprises independent fields for separately storing a first data size specifier for the memory and a second data size specifier for at least one general purpose register within the data processing system.

43. (previously presented) The data processing system of claim 41 wherein the control information of the first single instruction of the data processing instructions further comprises a field that specifies a storage location within the data processing system for defining a first data size specifier for the memory and a second data size specifier for at least one general purpose register within the data processing system.

44. (original) The data processing system of claim 41 further comprising control circuitry that adjusts data element size when necessary to communicate data when size of data elements stored in the memory differ from size of data elements stored in the at least one storage location in the data processing system external to the memory.